

TURBO DECODER AND TURBO INTERLEAVER

ABSTRACT OF THE DISCLOSURE

A processor on which a software-based interleaver is run performs interleaver generation, which is split into two parts to reduce the overhead time of interleaver changing. First, preprocessing prepares seed variables, requiring a small memory. Second, on-the-fly address generation generates interleaved addresses through simple adding and subtracting operations using the seed variables.

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